UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,287	04/01/2004	Soon-Il Ahn	8054-57 (LW9035US/KE)	8332

22150 7590 05/03/2006

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,287	AHN ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 1 April 2004. Claims 1-19 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Isobe et al. (2003/0218169).

Isobe et al. discloses a method for exposing a layer with a light where a mask including a pattern shape is formed over the layer formed on a substrate; and scanning the mask with the light, such that a direction of the scanning is substantially perpendicular to a longitudinal direction of the pattern shape to form a pattern (para. 29 & 92).

Referring to claim 2, wherein the pattern formed on the substrate is electrically coupled with a conductive pattern (111) disposed in a different layer from the pattern to generate a coupling capacitance, wherein an insulation layer (110) is disposed between the pattern and the conductive pattern (111) (para 87-90).

Referring to claim 3, wherein the pattern formed on the substrate corresponds to a data line (para. 90-92).

Referring to claim 4, forming an insulation layer (615) on the substrate having the data line; and forming a pixel electrode (670) as a conductive pattern on the substrate having the insulation layer (615), wherein a direction of scanning is substantially perpendicular to a longitudinal direction of the data line during an exposure process for forming the pixel electrode (670) (para. 29 & 159-163).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isobe et al. in view of Kim (2003/0211404).

Isobe et al. disclose the subject matter claimed above except the substrate corresponds to a substrate of a patterned vertical alignment mode liquid crystal display device having a size of nineteen inches and one cell is exposed by the mask.

Kim discloses a method for exposing a layer with a light where a mask including a pattern shape is formed over the layer formed on a substrate; and scanning the mask with the light to form a pattern (para. 17 & 18). Kim further discloses the substrate having a size of more than or equal to seventeen inches, wherein the substrate

corresponds to a substrate of a patterned vertical alignment mode liquid crystal display device having a size of nineteen inches (para. 10 and 14-16). Kim also discloses exposing one pattern (cell) using the mask (Fig. 4; para. 41).

Since Isobe et al. and Kim are both from the same field of endeavor, a method for exposing a layer with a light, the purpose disclosed by Kim would have been recognized in the pertinent art of Isobe et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Isobe et al. by the substrate corresponds to a substrate of a patterned vertical alignment mode liquid crystal display device having a size of nineteen inches and one cell is exposed by the mask as taught by Kim to increase the surface area of the liquid crystal display.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isobe et al. in view of Tanuma et al. (5,718,839).

Isobe et al. disclose the subject matter claimed above except an interval between the data line and a pixel electrode formed on the substrate being at least 6.25 μm.

Tanuma et al. disclose a method for exposing a layer with a light where a mask including a pattern shape is formed over the layer formed on a substrate; and scanning the mask with the light to form a pattern (Fig. 20b; col. 26, lines 39-54). Tanuma et al. further disclose an interval between the data line and a pixel electrode formed on the substrate is 10 μm or less (col. 8, lines 40-56).

Since Isobe et al. and Tanuma et al. are both from the same field of endeavor, a method for exposing a layer with a light, the purpose disclosed by Tanuma et al. would have been recognized in the pertinent art of Isobe et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Isobe et al. by an interval between the data line and a pixel electrode formed on the substrate being 10 μm or less as taught by Tanuma et al. to prevent abnormalities in the liquid crystals (col. 8, lines 40-56).

Claims 9, 10, 14, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (2003/0213966) in view of Isobe et al.

Yang et al. disclose a method of forming a thin film transistor substrate for a liquid crystal display device where a gate wiring layer is formed on a substrate (10); etching the gate wiring layer to form a gate wiring that includes a gate line (22), a gate pad (end) (24) and a gate electrode (26) (para. 235); forming a gate insulation layer (30) on the substrate (10) having the gate wiring formed on the substrate (10) (para. 236); forming a semiconductor layer pattern (40) and an ohmic contact layer pattern (50) on the gate insulation layer (30) in sequence (para. 236 & 237); forming a data wiring layer on the substrate (10) having the semiconductor layer pattern (40) and the ohmic contact layer pattern (50); forming a photoresist layer on the data wiring layer; disposing a mask including a pattern shape over the photoresist layer formed on the substrate (10); the mask with a light, such that a direction of the scanning is patterning the data wiring layer to form a data wiring including a data line (62) crossing the gate line (22), a data pad

(end) (68) connected to the data line (62), a source electrode (65) connected to the data line (62), and a drain electrode (66) in an opposite position to the source electrode (65) around the gate electrode(26) (para. 237 & 238); forming a protection layer (70) on the substrate (10) having the source and drain electrodes (65 &66) formed thereon; patterning the gate insulation layer (30) and the protection layer (70) to form contact holes (72, 74, 76, 78), the contact holes exposing the gate pad (end) (24), the data pad (end) (68) and the drain electrode (66), respectively (para. 239); forming a transparent conductive layer; and etching the transparent conductive layer to form an supplementary gate pad (auxiliary gate end) (84) being electrically connected to the gate pad (end) (24), a(n) supplementary data pad (auxiliary data end) (88) being electrically connected to the data pad (end) (68), and a pixel electrode (84) being electrically connected to the drain electrode (66) (para. 239 & 240). Yang et al. further disclose the photosensitive layer pattern including a first portion, a second portion thicker than the first portion, and a third portion thinner than the first portion (para. 140; claim 75). Yang et al. also disclose wherein the first portion is positioned between the source electrode and the drain electrode, and the second portion is positioned over an upper portion of the data wiring (para. 140).

Yang et al. do not disclose scanning substantially perpendicular to a longitudinal direction of the pattern shape to expose the photoresist layer.

Isobe et al. discloses a method for exposing a layer with a light to form a thin film transistor where a mask including a pattern shape is formed over the layer formed on a substrate; and scanning the mask with the light, such that a direction of the scanning is

substantially perpendicular to a longitudinal direction of the pattern shape to form a pattern (para. 29 & 92).

Since Yang et al. and Isobe et al. are both from the same field of endeavor, forming a thin film transistor, the purpose disclosed by Isobe et al. would have been recognized in the pertinent art of Yang et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yang et al. by canning substantially perpendicular to a longitudinal direction of the pattern shape to expose the photoresist layer as taught by Isobe et al. to prevent overlapping of the channel region (para. 28).

Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Isobe et al. as applied to claims 9 and 14 above, and further in view of Tanuma et al.

Yang et al. in view of Isobe et al. disclose the subject matter claimed above except an interval between the data line and a pixel electrode formed on the substrate being at least 6.25 μm.

Tanuma et al. disclose a method for exposing a layer with a light where a mask including a pattern shape is formed over the layer formed on a substrate; and scanning the mask with the light to form a pattern (Fig. 20b; col. 26, lines 39-54). Tanuma et al. further disclose an interval between the data line and a pixel electrode formed on the substrate is 10 μm or less (col. 8, lines 40-56).

Since Yang et al. and Tanuma et al. are both from the same field of endeavor, a method for exposing a layer with a light, the purpose disclosed by Tanuma et al. would have been recognized in the pertinent art of Yang et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yang et al. by an interval between the data line and a pixel electrode formed on the substrate being 10 μm or less as taught by Tanuma et al. to prevent abnormalities in the liquid crystals (col. 8, lines 40-56).

Claims 12, 13, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Isobe et al. as applied to claims 9 and 14 above, and further in view of Kim.

Yang et al. in view of Isobe et al. disclose the subject matter claimed above except the substrate corresponds to a substrate of a patterned vertical alignment mode liquid crystal display device having a size of nineteen inches and one cell is exposed by the mask.

Kim discloses a method for exposing a layer with a light where a mask including a pattern shape is formed over the layer formed on a substrate; and scanning the mask with the light to form a pattern (para. 17 & 18). Kim further discloses the substrate having a size of more than or equal to seventeen inches, wherein the substrate corresponds to a substrate of a patterned vertical alignment mode liquid crystal display device having a size of nineteen inches (para. 10 and 14-16). Kim also discloses exposing one pattern (cell) using the mask (Fig. 4; para. 41).

Since Yang et al. and Kim are both from the same field of endeavor, a method for exposing a layer with a light, the purpose disclosed by Kim would have been recognized in the pertinent art of Yang et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yang et al. by the substrate corresponds to a substrate of a patterned vertical alignment mode liquid crystal display device having a size of nineteen inches and one cell is exposed by the mask as taught by Kim to increase the surface area of the liquid crystal display.

Referring to claim 18, Kim discloses simultaneously exposing a plurality of cells using the mask (Fig. 5A; para. 44).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Zandra V. Smith
Supervisory Patent Examiner
27 April 2006